IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A signal processor comprising:

(1) a plurality of function blocks ~~for~~ configured to perform signal processing; ~~and~~

(2) a plurality of dedicated ~~output path~~ paths ~~for~~ configured to transmit ~~transmitting~~ debug information for debugging ~~for~~ the signal processor, the debug information obtained from ~~each of~~ respective function blocks of the plurality of function blocks; and

at least two of the dedicated paths provided for one of the plurality of function blocks, said paths configured to transmit input data and output data associated with said one of the plurality of function blocks.

Claim 2 (Currently Amended): The signal processor according to claim 1, wherein the dedicated ~~output path transmits~~ paths transmit the debug information serially.

Claim 3 (Original): The signal processor according to claim 1, wherein the debug information includes input data to at least one of the plurality of function blocks.

Claim 4 (Original): The signal processor according to claim 1, wherein the debug information includes output data from at least one of the plurality of function blocks.

Claim 5 (Original): The signal processor according to claim 1, wherein the debug information is data in an arbitrary length (size).

Claim 6 (Original): The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system,

wherein one of the plurality of function blocks is an error correction coder block, which inputs transmission data for coding as input data, performs error correction coding as the signal processing, and outputs a coded data series as output data.

Claim 7 (Original): The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is a modulator block, which inputs a coded data series as input data, performs modulation as the signal processing, and outputs modulated transmission data as output data.

Claim 8 (Original): The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is a demodulator block, which inputs received modulated data as input data, performs demodulation as the signal processing, and outputs a demodulated data series as output data.

Claim 9 (Original): The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is an error correction decoder block, which inputs a decoded data series as input data, performs error bit correction as the signal processing, and outputs decoded data as output data.

Claim 10 (Currently Amended): The signal processor according to claim 1, further comprising:

a selection multiplex output block ~~for acquiring~~ configured to acquire an instruction from an outside of the signal processor, ~~selecting~~ select the debug information based on the instruction acquired, ~~inputting~~ input the debug information selected via the dedicated output path, and ~~outputting~~ output the debug information inputted to the outside of the signal processor.

Claim 11 (Currently Amended): The signal processor according to claim 10, wherein the selection multiplex output block selects multiple pieces of debug information based on the instruction, inputs the multiple pieces of debug information, multiplexes the multiple pieces of debug information, and outputs multiplexed debug information to the outside of the signal processor.

Claim 12 (Original): The signal processor according to claim 11, wherein the multiple pieces of debug information are acquired from different function blocks.

Claim 13 (Original): The signal processor according to claim 10, wherein the selection multiplex output block performs time multiplexing.

Claim 14 (Original): The signal processor according to claim 1, wherein the debug information is added with time information.

Claim 15 (Original): The signal processor according to claim 14, wherein the time information is added by a function block.

Claim 16 (Original): The signal processor according to claim 15, wherein the time information includes a plurality of frame counters of different cycles.

Claim 17 (Original): The signal processor according to claim 16, wherein the plurality of frame counters includes CFN (Connection Frame Number Counter) and BFN (Node B Frame Number Counter).

Claim 18 (New): The signal processor according to claim 1, wherein the at least two dedicated paths comprise a first path configured to transmit the input data and a second path configured to transmit the output data.

Claim 19 (New): The signal processor according to claim 1, further comprising:

a memory disposed inside the one of the plurality of function blocks.

Claim 20 (New): The signal processor according to claim 1, further comprising:

at least one of a digital signal processor (DSP), a large scale integration (LSI) chip, and a field programmable gate array (FPGA) included in the plurality of function blocks.